tester time is saved compared with the case of prior art where the BIST has to restart from cycle 1 (as opposed to resuming) after the content of the location associated with each failing cycle is collected by scanning-out the entire the memory chip.

In the embodiments described above, the memory chip 120 (FIG. 1) has only two RAMs 140.1 and 140.2. In general, the memory chip 120 can have any number of RAMs. For example, assume the memory chip 120 has 2^N RAMS (N is a positive integer). As a result, the RAM select mux 137 needs to have 2^N inputs, the chip mux 150 needs to have 2^N inputs, and the RAM select register 136 needs to have N bits. Alternately, a chip could contain P BISTs 130, whereby not all SRAMs share the same BIST 130, and the number of SRAMs sharing a BIST 130 is less than N, in which case, the BIST multiplexer 137 would need to have less than N inputs. In this case however, the chip mux 150 would still require N inputs (one for each SRAM on the chip).

In the embodiments described above, the BIST state register 135 has 18 bits. In general, the BIST state register 135 can have any number of bits depending on how many bits of the outputs of the BIST control generator 132, the BIST address generator 133, and the BIST data generator 134 need to be saved so that the BIST 130 can resume later.

In the embodiments described above, the RAM 140.1 and 140.2 are 32 bits and 64 bits wide. In general, a RAM 140.1 can be K bits wide (K is positive integer). Then, if the BIST state register 135 has L bits (L is positive integer), the associated loop needs to be shifted K + L times at a pause.

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With the contents of the failing locations of the RAMs 140.1 and 140.2 collected by the tester 110, analysis can be done to identify the exact positions of the failing bits of these locations.

In FIG. 2, for simplicity, some existing connections are not shown. For instance, the connections 932, 933, and 934 from the BIST control generator 132, the BIST address generator 133, and the BIST data generator 134, respectively, are also connected (but not shown) to the memory array 142.2. The connection 934 from the BIST data generator 134 is also connected (but not shown) to the comparator 146.2 via connection 946.2.

In summary, for each RAM 140.i, the BIST 130 runs only two passes. During the first testing pass, the BIST 130 sequentially and without pause runs through a predetermined sequence of cycles while the tester 110 collects the cycle numbers of the failing cycles.

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During the second/last testing pass, the BIST 130 sequentially runs through the same cycles as in the first testing pass, but pauses at each failing cycle identified in the first testing pass so that the tester 110 can collects the content of the location associated with the failing cycle. In the example above, for the RAM 140.1, there are two failing cycles 2200d and 2400d identified during the first testing pass. As a result, during the second testing pass, the BIST 130 pauses a first time for 50 clocks for the tester 110 to collect the content of the location associated with the failing cycle 2200d, and pauses a second time for 50 clocks for the tester 110 to collect the content of the location associated with the failing cycle 2400d. In general, for the RAM 140.1, if M (a positive integer) failing cycles are identified during the first testing pass, then during the second testing pass, the BIST 130 pauses M times for 50 clocks per pause. As a result, a lot of